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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,604	10/28/2003	Mark W. Morgan	TI-36312 / DDM03-022	6318

23494 7590 02/23/2005

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EXAMINER

TRA, ANH QUAN

ART UNIT	PAPER NUMBER
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2816

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/695,604

Applicant(s)

MORGAN ET AL.

Examiner

Quan Tra

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 January 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 01/17/05. A new ground of rejection is introduced.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-9, 11 and 14-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujioka (USP 6020781).

As to claim 1, Fujioka discloses in figure 1 an apparatus comprising: (the limitation “for regulating voltage for at least one differential transistor pair having a voltage follower buffer; the voltage follower section having a first voltage-temperature response” is merely a statement of intended use as such, not given any patentable weight) a differential amplifier (61, 63) having two input loci (positive and negative input terminals of 61) and an output locus (drain of 63); a first input locus (negative input terminal) of the two input loci receiving a reference voltage (VREF); a temperature responsive unit (64-66) coupled between the output locus and ground; and a feedback line coupled between temperature responsive unit and a second input locus (positive input terminal) of the two input loci; the temperature responsive unit having a second voltage-temperature response similar to the first voltage-temperature response (it is inherent that elements 64-66 has voltage temperature response. Elements 64-66 are capable of provide

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voltage-temperature response that is similar to a voltage temperature response of the intended use circuit that is supplied by Fujioka's regulator circuit).

As to claim 2, figure 1 shows the temperature responsive unit comprises at least two resistive devices (65, 66) and a temperature sensitive diode (64) device coupled in series.

As to claim 3, figure 1 shows that one resistive device of the at least two resistive devices is coupled with ground.

As to claim 4, figure 1 shows that the temperature sensitive diode device is coupled with ground (via 65, 66).

As to claim 5, figure 1 shows that the temperature sensitive diode device is coupled with the output locus.

As to claim 6, figure 1 shows that the feedback line is coupled with the temperature responsive unit at a connection locus; the connection locus being separated from ground by at least one resistive device (66) of the at least two resistive devices and separated from the output locus by at least one resistive device (65) of the at least two resistive devices.

As to claim 7, figure 1 shows that one resistive device (66) of the at least two resistive devices is coupled with ground.

As to claim 8, figure 1 shows that the temperature sensitive diode device is coupled with ground (via 65, 66).

As to claim 9, figure 1 shows that the temperature sensitive diode device is coupled with the output locus.

As to claim 11, figure 1 shows that one resistive device of the at least two resistive devices is coupled with ground.

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Claims 14-19 recite similar limitations of claims 1-13. Therefore, they are rejected for the same reasons.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 10, 12, 13 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujioka (USP 6020781) in view of Cartwright (USP 4064506)

Fujioka's figure 1 shows all limitations of the claims except for the diode device is diode coupled bipolar transistor. However, Cartwright teaches in column 5, lines 35-47, that bipolar transistors have an advantage over FET's in that their transconductances tend to be little affected by emitter-to-collector potential variations. Therefore, it would have been obvious to one having ordinary skill in the art to use bipolar transistors for Fujinoka's transistors for the purpose of improving the performance of the voltage reference voltage generator.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Quan Tra', with a stylized, flowing script.

Quan Tra
Primary Examiner

February 18, 2005